Claims

[c1] What is claimed is:

1.A method of fabricating a flash memory cell, the method comprising:

providing a substrate, that comprises a channel region and a bit line region in its surface;

forming a stacked layer on the substrate in the channel region, wherein the stacked layer comprises a polysilicon layer and a sacrificial layer formed on the polysilicon layer;

depositing a dielectric layer to cover the channel region and the bit line region, the top surface of the dielectric layer on the surface of the substrate within the bit line region being above the top surface of the polysilicon layer and below the top surface of the sacrificial layer;

isotropically etching away a predetermined thickness of the dielectric layer to expose a portion of the sacrificial layer, and, at the same time, dividing the dielectric layer into a first portion dielectric layer positioned on the sacrificial layer and a second portion dielectric layer that is not connected with the first portion dielectric layer; and

removing the sacrificial layer and the first portion dielectric layer.

[c2] 2.The method of claim 1 wherein the dielectric layer is an HDP (high density plasma, HDP) oxide layer.

[c3] 3.The method of claim 1 wherein the substrate further comprises a doped region adjacent to the polysilicon layer in the bit line region, the doped region serves as a buried source (BS) or a buried drain (BD).

[c4] 4.The method of claim 1 wherein the sacrificial layer comprises silicon nitride.

[c5] 5.The method of claim 1 wherein the second portion dielectric layer has a protrusion structure near the polysilicon layer that is able to increase GCR (gate coupling ratio) of the flash memory.

[c6] 6.The method of claim 1 wherein the sacrificial layer is removed by using wet etching.

[c7] 7.The method of claim 1 wherein the predetermined thickness ranges between

450 and 750 angstroms.

[c8] 8.The method of claim 1 wherein the predetermined thickness is about 600 angstroms.

[c9] 9.A method for eliminating HF acid corrosion during a flash memory fabrication process and reducing random bit failures of the flash memory, the method comprising:

providing a substrate having a channel region and a bit line region thereon;

forming a stacked layer on the substrate in the channel region, wherein the stacked layer comprises a first polysilicon layer and a sacrificial layer formed on the first polysilicon layer;

depositing a dielectric layer to cover the channel region and the bit line region;

isotropically etching away a predetermined thickness of the dielectric layer to expose a portion of the sacrificial layer, and, at the same time, dividing the dielectric layer into a first portion dielectric layer positioned on the sacrificial layer and a second portion dielectric layer that is not connected with the first portion dielectric layer;

removing the sacrificial layer;

depositing a second polysilicon layer over the first polysilicon layer such that the first and second polysilicon layers constitute a floating gate for the flash memory;

forming an ONO film over the floating gate; and

forming a third polysilicon layer over the ONO film.

[c10] 10.The method of claim 9 wherein the top surface of the dielectric layer on the substrate within the bit line region is above top surface of the polysilicon layer and below top surface of the sacrificial layer.

[c11] 11.The method of claim 9 wherein the dielectric layer is an HDP(high density plasma, HDP) oxide layer.

[c12] 12.The method of claim 9 wherein the substrate further comprises a doped region adjacent to the polysilicon layer in the bit line region, the doped region serves as a buried source (BS) or a buried drain (BD).

[c13] 13.The method of claim 9 wherein the sacrificial layer is composed of silicon nitride.

[c14] 14.The method of claim 9 wherein the second portion dielectric layer has a protrusion structure near the first polysilicon layer that is able to increase GCR (gate coupling ratio) of the flash memory.

[c15] 15.The method of claim 9 wherein the sacrificial layer is removed by using wet etching.

[c16] 16.The method of claim 15 wherein the sacrificial layer is removed by using hot phosphoric acid.

[c17] 17.The method of claim 9 wherein the predetermined thickness ranges between 450 and 750 angstroms.

[c18] 18.The method of claim 17 wherein the predetermined thickness is about 600 angstroms.